Application No. 09/252,551

Please cancel Claims 104 - 132, 136 - 140, 145, 146, 152, 154 - 170.

Please amend Claims 133, 135, 141, 147 and 153 as set forth in amended form below:

104 ~~133~~. (twice amended) A bidirectional data communication system comprising:

communication signals having individual ones of a plurality of analog levels to represent information;

a plurality of signal lines disposed in pairs and defining a multi-pair communication environment, each signal line transmitting or receiving said communication signals;

a transmitter block, including a plurality of transmitters, each coupled to particular ones of the signal line pairs;

a receiver block, including a plurality of receivers, each coupled to particular ones of the signal line pairs, each receiver including;

an analog to digital converter configured to convert a plurality of analog levels into a corresponding plurality of digital levels defining a digital signal; and

a fully digital adaptive equalizer coupled to the analog to digital converter and operating on the digital signal to define information represented by the plurality of digital levels;

the receiver block further comprising timing recovery circuitry coupled to receive the digital signal from the analog to digital converter and extract timing information therefrom, the analog to digital converter operatively responsive to said timing information and performing digital conversions at a rate defined thereby;

wherein the communication signals are provided in packets, each packet comprising a preamble portion and a data

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containing portion, the preamble portion including timing signals; and

wherein the timing recovery circuitry comprises a first timing loop having a high gain stage and a second timing loop having a low gain stage, the first timing loop locking the analog to digital converter in phase with the preamble portion the second timing loop locking the analog to digital converter in phase with the data containing portion.

~~135~~106. (twice amended) A bidirectional data communication system comprising:

communication signals having individual ones of a plurality of analog levels to represent information;

a plurality of signal lines disposed in pairs and defining a multi-pair communication environment, each signal line transmitting or receiving said communication signals;

a transmitter block, including a plurality of transmitters, each coupled to particular ones of the signal line pairs;

a receiver block, including a plurality of receivers, each coupled to particular ones of the signal line pairs, each receiver including;

an analog to digital converter configured to convert a plurality of analog levels into a corresponding plurality of digital levels defining a digital signal; and

a fully digital adaptive equalizer coupled to the analog to digital converter and operating on the digital signal to define information represented by the plurality of digital levels;

the receiver block further comprising timing recovery circuitry coupled to receive the digital signal from the analog to digital converter and extract timing information therefrom, the analog to digital converter operatively responsive

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to said timing information and performing digital conversions at a rate defined thereby;

the digital adaptive equalizer further comprising:

a feed forward equalizer having an input receiving the digital signal from the analog to digital converter and an output;

a slicer coupled to receive the digital signal from the feed forward equalizer and outputting a signal representing a symbol, the signal characterized by the digital levels;

an adder disposed between the feed forward equalizer and the slicer; and

a decision feedback equalizer having an input receiving the signal output by the slicer and an output coupled to the adder, the adder summing the output of the decision feedback equalizer with the output of the feed forward equalizer.

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~~141~~. (twice amended) A bidirectional data communication system comprising:

communication signals having individual ones of a plurality of analog levels to represent information;

a plurality of signal lines disposed in pairs and defining a multi-pair communication environment, each signal line transmitting or receiving said communication signals;

a transmitter block, including a plurality of transmitters, each coupled to particular ones of the signal line pairs;

a receiver block, including a plurality of receivers, each coupled to particular ones of the signal line pairs, each receiver including;

an analog to digital converter configured to convert a plurality of analog levels into a corresponding plurality of digital levels defining a digital signal;

an automatic gain control circuit coupled in feedback fashion to the analog to digital converter and operatively responsive to output signals therefrom to control the gain of received communication signals; and

a fully digital adaptive equalizer coupled to the analog to digital converter and operating on the digital signal to define information represented by the plurality of digital levels;

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the digital adaptive equalizer further comprising:

a feed forward equalizer having an input receiving the digital signal from the analog to digital converter and an output;

a slicer coupled to receive the digital signal from the feed forward equalizer and outputting a signal representing a symbol, the signal characterized by the digital levels;

an adder disposed between the feed forward equalizer and the slicer; and

a decision feedback equalizer having an input receiving the signal output by the slicer and an output coupled to the adder, the adder summing the output of the decision feedback equalizer with the output of the feed forward equalizer.

111 ~~147~~. (amended) In a bidirectional communication system, a method of processing signals received through a multi-pair transmission medium, the signals having characteristic values occurring at a characteristic frequency, the method comprising:

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providing an A/D converter, coupled to receive the signals from the transmission medium;

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providing a sampling clock signal at a sampling clock frequency equal to the characteristic occurrence frequency of received signal characteristic values;

sampling the received signals in the A/D converter at the sampling clock frequency;

generating signal samples at the sampling clock frequency, each signal sample being output from the A/D at a time assumed to correspond to the occurrence of a signal characteristic value;

processing each signal sample in a timing recovery circuit coupled, in feedback fashion, between the output of the A/D and a sampling clock input thereto;

determining whether the occurrence of a signal characteristic value leads or lags the sampling clock signal in phase; and

adjusting the phase of the sampling clock signal such that each signal sample is output from the A/D at a time that actually corresponds to the occurrence of a signal characteristic value, a sampling clock phase thereby being locked to a corresponding phase of a signal characteristic value;

wherein the received signals are analog signals disposed in packets, each packet of the analog signals disposed in packets being divided into a first packet region comprising timing signals and a second packet region comprising data signals, the method further comprising:

sampling the received data signals in the A/D converter at the sampling clock frequency, wherein the data signals are sampled after the phase of the sampling clock signal has been locked to the phase of a signal characteristic value of the timing signals.

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153. (amended) In a bidirectional communication system, a method of processing analog signal packets received through a multi-pair transmission medium, each analog signal packet including a plurality

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of signals having characteristic values occurring at a characteristic frequency, the method comprising:

providing a sampling clock signal at a sampling clock frequency equal to the characteristic occurrence frequency of received signal characteristic values;

predicting an occurrence time corresponding to the characteristic occurrence frequency of received signal characteristic values;

sampling the received signals at the sampling clock frequency and at the predicted occurrence time to thereby generate signal samples at the sampling clock frequency, each signal sample assumed to correspond to the occurrence of a signal characteristic value;

processing the signal samples in a high gain error generator, the high gain error generator determining whether the occurrence of a signal characteristic value leads or lags the sampling clock signal in phase; and

adjusting the phase of the sampling clock signal such that each signal sample is generated at a time that actually corresponds to the occurrence of a signal characteristic value, the sampling clock having an occurrence time locked in phase with a corresponding occurrence of a signal characteristic value;

the signals of each analog signal packet being characterized by a plurality of analog amplitude values, the values of the analog amplitudes defining information content, the method further comprising:

dividing each analog signal packet into a first packet region comprising timing signals and a second packet region comprising data signals; and

converting the analog amplitude values of the data signals to digital representations thereof by an A/D converter after the occurrence time of the sampling clock signal has been locked to the

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